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MOSFET Scaling to Sub-Micron Range; Annalysis of Characteristic Curves in Relation to Device Parameters

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***Abstract*-The advances in Silicon technology have driven the MOSFET device fabrication towards submicron regime. This work presents simulated results where gate dimensions are determined and associated parameters are defined. NMOSFET with gate lengths 100Å, 65Å, 42.25Å, 27.27Å and 17.85Å, gate width of 100Å and with oxide thickness of 2Å were studied. All the simulations were done using MATHCAD and the results obtained were then used to plot characteristic curves and the transfer curves using ORIGIN lab software. From the results of characteristic curves it was observed that at V_G=0V there was no conducting channel between the source and the drain. When a small V_D is applied, and as long as the V_D is small, enough not to cause any significant difference in the surface potential near source and drain, the electron concentration throughout the channel remains the same and channel behaves like a resistor. As V_D is increased the potential drop across the channel reduces the voltage between the gate and the inversion layer near the drain and as a result the electron concentration in the channel near drain decreases causing increase in the channel resistance and therefore I_D-V_D bends. When gate bias was increased from V_{G1} to V_{G2} (where V_G represents the gate voltage) it causes an increase in the inversion layer charge and hence channel resistance reduces causing a larger drain current for a given V_D. As the dimensions are scaled down, the drain current increases, evidence that sub-micron devices have better performance as compared to un-scaled devices. It can also be noted that there is a strong correlation between device dimensions and device performance. This shows that sub-micron device has better performance as compared to un-scaled device. *Keywords*- MOSFET, short channel effects, velocity overshoot, DIBL, CMOS.**

I. Introduction

The MOSFET is a three terminal device which has many applications both in analog and digital electronics [1]. In silicon MOSFET, the gate contact is separated from the channel by an insulating silicon dioxide (SiO_2) layer. The charge carriers of the conducting channel constitute an inversion charge, that is, electrons in the case of a p-type substrate (n-channel device) or holes in the case of an n-type substrate (p-channel device), induced in the semiconductor at the silicon-insulator interface by the voltage applied to the gate electrode [2].

The electrons enter and exit the channel at n+ source and drain contacts in the case of an n-channel MOSFET, and at p+ contacts in the case of a p-channel MOSFET [3-5]. MOSFETs are used both as discrete devices and as active elements in digital and analog monolithic integrated circuits (ICs).

II. Theory

In recent years, the device feature size of such circuits has been scaled down into the deep sub-micron range which comes with a commensurate increase in speed and in integration scale [6]. Hundreds of millions of transistors on a single chip are used in microprocessors and in memory ICs today [2]. CMOS technology combines both n-channel and p-channel MOSFETs to provide very low power consumption along with high speed. Aggressive scaling of the thickness of the gate insulator in CMOS transistors has caused the quality and reliability of ultrathin dielectrics to assume greater importance [7-10]. Very important issues in this development are the increasing levels of complexity of the fabrication process and the many subtle mechanisms that govern the properties of these deep sub-micron FETs [4]. One of the application areas of CMOS is in analog circuits, spanning a variety of applications from audio circuits operating at the kilohertz (kHz) range to modern wireless applications operating at gigahertz (GHz) frequencies.

III. Methodology

This study was conducted through device simulation. The study was concerned with investigating the effect of scaling MOSFET gate dimensions on the performance of the device. It is specifically intended to investigate the relationship between saturation drain current against saturation drain voltage at different scaling factors. This method enables the researcher to manipulate the gate dimensions and study/observe the resulting effects. This simulation research design entails, inputting the parameters required, systematic manipulation of some characteristics and examination of the outcome.

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All simulations were done using MATHCAD software. NMOSFET with gate lengths 100Å, 65Å, 42.25Å, 27.27Å and 17.85 Å, gate widths 100Å and with oxide thickness of 2Å were studied. A gate length of 100 Å was chosen as a very large device and has been scaled by a factor of k, k^2, k^3, k^4 where $k = 0.65$. The results obtained were then used to plot the graphs using ORIGIN lab software at. Assuming doping concentration N_a in the P substrate region, the gate voltage (V_G), drain voltage (V_D), built in voltage (V_d), gate length (L), gate width (Z), electron charge (e) and electron mobility (μ_n) then the following equations were used to simulate the results;

$$I_{DS} = KV_{DS}^2 = K(V_G - V_T)^2$$

Where

$$K = \frac{\in \mu_n Z}{2La}$$

This gives the change in drain current $I_{DS,sat}$ with the drain voltage $V_{DS,sat}$ at different scaling factors.

IV. Results And Discussions

This chapter contains the results of all simulations done. Figures 1 to 5 shows the graphs of drain current against drain voltage at different gate voltage and with different scaling factors.

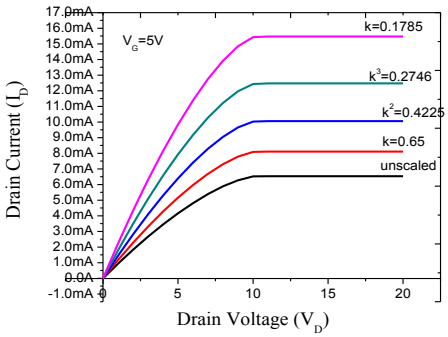

Figure 1: Graph of I_D verses V_D at V_G=5V for different scaling factors (un-scaled, K=0.65, k^2=0.4225, k^3=0.2746 and k^4=0.1785)

From figure 1 it shows a graph of drain current against drain voltage at V_G=5V and at different scaling factors as shown above. For un-scaled device at gate length of 100Å, and gate width of 100Å the current output is slightly small. As we scale by a factor of k=0.65, k^2, k^3 and k^4 the current increases.

As drain voltage increases, the drain current also increases but reaches a nearly constant value where any further increase in the drain voltage has no significant in the drain current and the device is said to be in saturation.

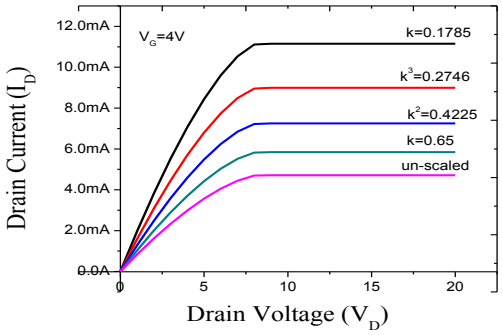

Figure 2: Graph of I_D verses V_D at V_G=4V for different scaling factors (un-scaled, k=0.65, k^2=0.4225, k^3=0.2746 and k^4=0.1785)

Figure 2 shows characteristic curves at V_G=4V and at different scaling factors. It is clearly observed that the output current increases with scaling.

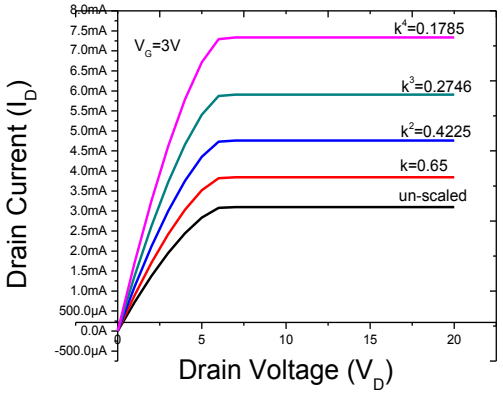

Figure 3: Graph of I_D verses V_D at V_G=3V for different scaling factors (k=1, k=0.65, k^2=0.4225, k^3=0.2746 and k^4=0.1785)

Figure 3 shows I_D-V_D characteristic curves for a device at V_G=3V and at different scaling factors as shown above. The current increases with scaling. From figures 1, 2 and 3 it is observed that as V_G is reduced the output current also reduces at the same voltage.

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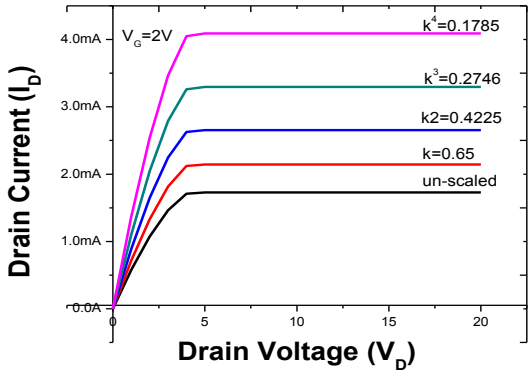

Figure 4: Graph of I_D versus V_D at V_G=2V for different scaling factors (k=1, k=0.65, k^2=0.4225, k^3=0.2746 and k^4=0.1785)

Figure 4 shows the characteristic curve at V_G=2V and at different scaling factors. It's also observed that the current output increases with scaling. Its observed here that a decrease in the gate voltage leads to a decrease in the output current this is attributed to the decrease in the inversion layer charge along the channel and hence the channel resistance increase causing a decrease in the current output.

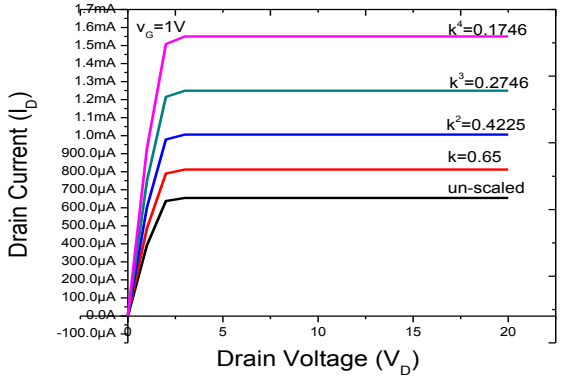

Figure 5: Graph of I_D versus V_D at V_G=1V for different scaling factors (k=1, k=0.65, k^2=0.4225, k^3=0.2746 and k^4=0.1785)

Figure 5 shows the characteristic curve for a device at V_G=1V and at different scaling factors. It's noted that the curves reaches saturation at a rather smaller drain voltages. The output current is noted to be small as gate voltage is reduced. This is because of reduction in the inversion layer charge and hence an increase in the resistance along the channel.

V. CONCLUSIONS

The findings indicated that for a miniaturized device there was quite an improvement on its performance. It's also observed that for a MOSFET with large geometry the drain current is significantly small but can be increased by scaling down the device. This shows that there is a strong correlation between device dimensions and device performance. This owes to the reduction in parasitic capacitances hence a higher speed. MOSFET current is dependent upon the carrier density in the channel. For Long channel devices, driving ability depends on channel length. The shorter the gate length, the greater the driving ability. This is because channel resistance is proportional to channel length. As a consequence, performance of the MOSFET can be enhanced by downscaling.

REFERENCES

[1] Ytterdal T., Cheng Y. and Fjeldldy T. A., "Device Modeling for Analog and RF CMOS Circuit Design," John Wiley and Sons Ltd, 2003

[2] Rashid, M. H., "Power Electronics: Circuits, devices, and applications," Pearson/Prentice Hall, 2004

[3] Jim´enez-Molinos F, G´amiz F, Palma A, Cartujo P and L´opez-Villanueva J A , 2002, Direct and trap-assisted elastic tunneling through ultrathin gate oxides J. Appl. Phys. **91** 5116–24

[4] Yu, B. et al, Short-Channel Effect Improved by Lateral Channel-Engineering in Deep-Submicronmeter MOSFET's,IEEE Transaction on electron devices, VOL. 44, NO. 4, April 1997.

[5] Lo S-H, Buchanan D. A., Taur Y. and Wang W. Quantum-mechanical modeling of electron tunneling current from the inversion layer of ultra-thin-oxide nMOSFETs IEEE Electr. Dev. Lett. **18** 209–11, 1997

[6] Roy, K. et al, Leakage Current Mechanisms and Leakage Reduction Techniques in Deep-Submicrometer CMOS Circuits, IEEE, VOL.91, NO. 2, Feb. 2003.

[7] Suzuki M., Murase K., Kato N., Togashi M., and Shirayama M., ''Advantages of metallic Amorphous Silicon Gate Applications,'' IEEE Trans. Electron Devices, Vol. ED-33, p.919,1986

[8] Choi, C-H. et al, Gate Length Dependent Polysilicon Depletion Effects, IEEE Electron Letters, VOL. 23, NO. 4 APRIL 2002.

[9] W. Quin et al, A Velocity Overshoot Subthreshold Current Model for Deep-Submicrometer MOSFET Devices.

[10] Liu, Z. et al,Threshold Voltage Model for Deep-Submicrometer MOSFET's, IEEE Transactions on Electron Devices, VOL. 40, NO. 1,Jan. 1993.

[11] http://www.ijarcsse.com/docs/papers/Volume_3/8_August 2013/V3I7- 0560.pdf

[12] Van der Meer, P. R. Van Staveren, A. Van Roermund, A. H. M., 2004. Low-Power Deep Sub-Micron CMOS Logic: Subthreshold Current Reduction. Dordrecht: Springer, p.78.

[13] Yannis Tsividis, 1999. Operational Modeling of the MOS Transistor, Second Edition, New York: McGraw-Hill.

[14] Eicke R. W., Jarek D., 2004. Predictive Simulation of Semiconductor Processing: Status and Challenges. Dordrecht: Springer.

[15] Jean-Pierre Colinge, Cynthia A. Colinge, 2002. Physics of Semiconductor Devices. Dordrecht: Springer.

[16] Kaushik Roy, Kiat Seng Yeo, 2004. Low Voltage, Low Power VLSI Subsystems. McGraw-Hill Professional, Fig. 1.1, p. 4.