Design and Implementation of a Low Cost High Bandwidth Sampling Bridge

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Abstract

Research involving high bandwidth signals in GHz range is limited in Kenyan Universities due to lack of high bandwidth measurement equipment such as sampling oscilloscopes and spectrum analyzers among others. The cost of these instruments from international vendors is very high and hence there is need to come up with low-cost alternatives in order to promote and enhance research in our local institutions. In this work the concept of high frequency sampling bridge is to be developed for high frequency measurements. Various sampling techniques and architectures have been studied and implemented with the idea of improving the bandwidth, sampling rate, rise time, bridge circuit design, reduction of noise and distortion, minimizing aperture errors, as well as reducing the overall design cost of the bridge. This work employs the Equivalent Time Sampling Technique (ETST) in order to minimize the cost of electronic devices at the output stage. The design is implemented on monolithic GaAs which generates fast pulses for sampling, Schottky diodes which are well suited for high frequency operations and SiGe HBT technology which require small implementation area thus compact light weight and low cost device. The implemented system is capable of sampling picoseconds signals at analog measurement bandwidth of 6 GHz or above with a rise time in the order of 100 ps with low noise and low distortion.

Keywords: *Bandwidth, Sampling Bridge, rise time, distortion, aperture error, signal, Equivalent Time Sampling Technique (ETST).*

Introduction

In order to achieve high resolution in measurement equipment such as microwave and laser radars, short picoseconds pulses are utilized. Since such pulses have a broad spectral content, their parameters are usually determined using high bandwidth sampling oscilloscopes which come at a high cost.

A sample is taken at every repetitive trigger event of a sampling oscilloscope and the sampled value stored in the sampling module. Through a low frequency path, the value is passed to the oscilloscope's display. The input signal frequency is only seen by the sampling module or the input stage after which the reconstructed signal passes through relatively low bandwidth amplifiers.

Attenuators trigger pickoff and protection devices in the sampling module do limit high bandwidth capacity capability and therefore should be avoided. The high bandwidth requirements necessitate sampling modules with components that are very sensitive to relatively small amplitude levels [1] – [5].

Given these requirements for the sampling oscilloscope coupled with high efficiency required in measurements of broadband analog signals, there necessitates a better alternative that is, to design a sampling bridge. Also the complexity of the circuitry requirement involved results in the cost of the sampling oscilloscope being very high.

This paper focuses on those mechanisms capable of exploiting the design related constraints and thus find optimum solutions to implement a low cost high bandwidth sampling bridge. The key specifications for consideration in the study of sampling ADCs include Distortion, noise, distortion plus noise, effective number of bits, bandwidth (full power and small signal) and sampling rate. Further in the Modern Trends the following are key considerations [4]

- Low Power: CMOS, Bi-MOS, or XFCB Processes
- Low Voltage: +/-5 V, +5 V, +5 V (Analog) / +3 V (Digital)
- Input Voltage Ranges not always Ground-Referenced
- Analog Input Can Generate Transient Currents.

Sample and Hold Amplifier

A typical sample and hold amplifier (SHA) has the following components [2]: the input amplifier, energy storage device (capacitor), output buffer, and switching circuits as shown in Figure 1

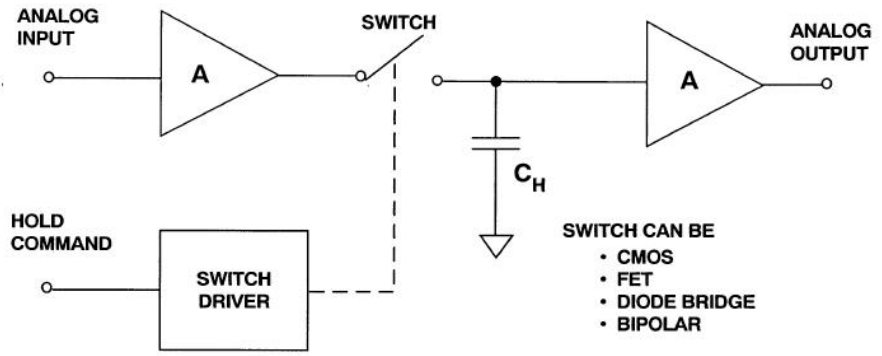

Figure 1: The basic Sample and Hold operation

The capacitor C_H is the energy storage device and the heart of the SHA. The input to the SHA is buffered by the input amplifier, which presents high impedance to the signal source, providing current gain to charge the hold capacitor.

During track mode, the voltage on the hold capacitor C_H follows (or tracks) the input signal with some delay and bandwidth limiting. When the switch is opened during hold mode, the capacitor retains the voltage present before it was disconnected from the input buffer. The output buffer offers high impedance to the hold capacitor to keep the held voltage from discharging prematurely. The switching circuit (which can be Bipolar, Diode Bridge, CMOS or FET) and its driver form the mechanism by which the SHA is alternatively switched between track and hold modes.

Diode Bridge Design For Wide Band ApplicationS

A sample and hold amplifier samples the input signal voltage before quantization. In this design, classic high-speed Schottky Diode Bridge has been used to isolate the output from the input and a hold capacitor to store the held voltage as shown in figure 2. During the track mode, transistor Q_1 is on and thus current I_1 flows through the diode bridge D_1, D_2, D_3 and D_4 which are forward biased and with low impedance towards flow of current, resulting in $V_a = V_{in}$ but with slight delay.

Transistor Q_1 turns off during the hold mode and Q_2 turns on by the action of the clock. The current from I_1 is directed around the diode bridge and since Q_1 is off, I_1 combines with I_2 at node *d* thus forward biasing the clamp diodes D_5 and D_6 and reverse biasing the diode bridge. This disconnects V_a from the input and its value maintained and stored on the hold capacitor C_h [7].

Figure 2 Diode bridge with unity gain output and bootstrap buffers.

The diode bridge requires a supply current of approximately 14 mA by the current sources I_1 and I_2 in Figure 2, for effective operation of the Track and Hold Amplifier (THA). At high frequencies, the impedance of these current sources needs to remain large in order to minimize the distortion of the bridge and extend the sampling frequency. This will also reduce the switching time of the circuit.

A comparison on current source technologies is made between pMOS and Si/ SiGe HBT. The pMOS current source transistor exhibits inherently large drain-gate and drain-substrate capacitance which makes it difficult to store and

maintain high impedance of a circuit at microwave

frequencies as $Z \propto \frac{}{jwC}$.

Reduced current source impedance reduces the input bandwidth and also lowers the bridge aperture. As a result, pMOS current sources would not be effective at high input bandwidths.

The technology in Si/SiGe HBT gives high quality factor inductors which provide the possibilities of implementing series inductance to increase the impedance of the circuit at high frequencies, as a result, improving the overall performance.

Therefore, implementing a series L-R current source circuit increases the impedance at higher frequencies and simulations demonstrate that the switching speed, analog input bandwidth, peak sampling rate and distortion of the diode bridge are improved through use of this approach [10] – [22].

Equivalent Time Sampling Technique.

The process of converting a portion of an input signal into a number of discrete electrical values for the purpose of storage, processing and/or display is called

Sampling. Sampling means that the continuous-time signal is replaced by a train of impulses. The value of each sampled signal is equal to the amplitude of the continuous input signal at the instant in time at which the signal is sampled [4].

There are a number of different implementations of sampling technology. The two methods mainly used by today's oscilloscopes are Real time sampling and Equivalent time sampling. The Equivalent time sampling can further be divided into sequential and random sampling.

Real time sampling works such that the sampler operates at maximum speed to acquire maximum number of points as possible in one sweep along the continuous signal. This sampling technique is intended to capture single shots or rather transient events. The sample rate required to actually digitize high frequency transients' events and the high speed memory required to store the waveform once digitized presents a great challenge for digital oscilloscopes.

The fact that many if not most of naturally occurring and man-made events are generally repetitive presents a platform for application of Equivalent Time Sampling Techniques (ETST). ETST takes advantage of this in that samples may be acquired over many repetitions of the signal, with one or more sample taken on each repetition.

In the case of sequential sampling the sampling gate pulse is shifted after each sampling cycle by a suitable small time interval ΔT, while in random sampling, this time intervals ΔT are not constant but follow in a statistical sequence. That is why a ΔT circuit is vital in this implementation**.**

Random equivalent time sampling is most common as it allows display of the input signal prior to the trigger point, without the use of a trigger line. Sequential equivalent time sampling provides much greater resolution and accuracy. Both techniques require the signal being repetitive.

The principle of sequential equivalent time sampling is illustrated in figure 3 adopted from [5]. This sampling technique is very useful when broadband pulses (150 ps) are to be recorded and amplified. It is much easier to extend such a signal by sequential sampling then deal with lower frequency sampled signal, than dealing directly with Ultra Wide Band signal. The electrical expenditure is relatively low [6] – [8].

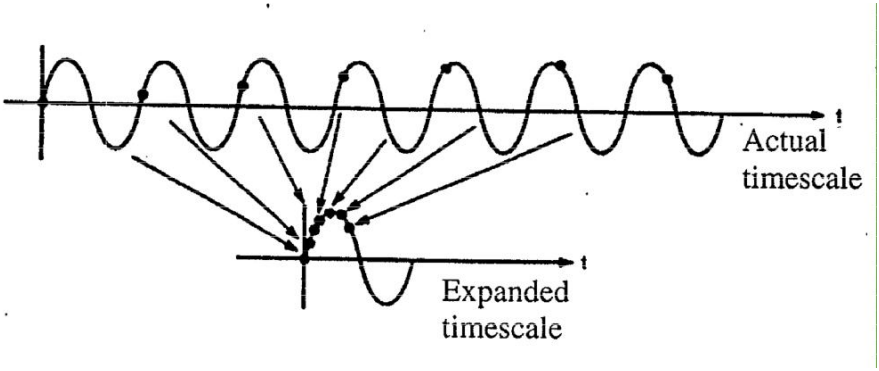

Figure 3: The principle of sequential equivalent time sampling. ΔT circuit

The ΔT circuit is an important part in sampling [5]. It consists of fast RC circuit and a slow RC circuit. The ΔT circuit shifts the pulses after each sampling event by a small time interval ΔT.

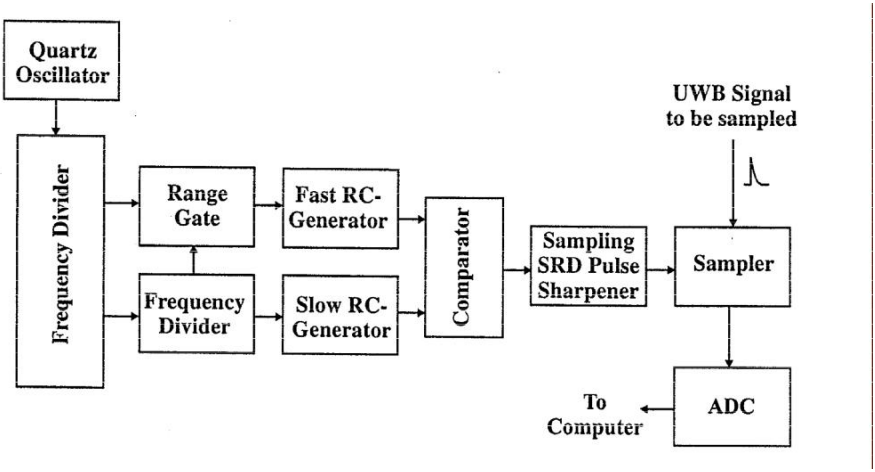

Figure 4: Block diagram of a sequential sampling system

Figure 4 represents a block diagram of a sequential sampling system [5] with ΔT circuit incorporated. The output of the first frequency divider controls a fast RC generator with a given time constant and a second frequency divider converts the frequency to Hz ranges. This second frequency divider controls a slow RC generator with a given time constant. The outputs of the two RC generators are compared by a comparator which produces a pulse when the voltages are equal. The pulse is then fed into the SRD sharpening circuit and used for sampling.

Since the controlling of the signal of the sampling pulses comes from the ΔT generator, where each clock signal is shifted a fixed shift ΔT of say 6 ns, a sequential sampling technique known as extended- time sampling would be realized. This operation will cause the sample output to be extended by a factor of 10_6 in time domain or to be down converted in frequency ranges from the GHz to KHz range. Therefore it would be possible to use simple operational amplifiers and reduce the number of high frequency components needed and as well reduce the cost of the sampler. On the other hand this KHz range signal could be converted to a digital signal using the A/D converter, and then we can apply signal processing techniques [9].

Experimental Results

The approach adopted in the design of the sampling bridge for high bandwidth applications i.e. applying the ETST and improved current sources results in improved input analogue bandwidth of 6 GHz or above and sampling picoseconds signals with rise time in the order of 100 ps, as well as an output with low noise and distortion. The bridge circuit design is relatively improved since current electronic components with low noise and high frequency capability will be used in implementation. Preliminary simulations indicate that the aperture errors, droop rate, delay error and distortion are relatively

minimized. The sampling technique used, (ETST) minimizes the cost of implementation electronics at the output stage.

Conclusion

The design for a track and hold circuit has been improved achieving wid-er bandwidth and lower distortion than previous circuits implemented in silicon technology, with performance comparable to the best GaAs-based track-and-holds. A standard diode-bridge design is used with ETST and an improved current source approach using series inductive loading to reduce the aperture time and lower distortion and to extend performance to higher frequencies.

The aspects of the ΔT circuit design at high frequencies were analyzed. The circuit exhibits input analog bandwidth in excess of 6 GHz. This circuit can be used as a building block for next-generation ultra wide bandwidth satellite communication systems and high bandwidth measurement equipments to enhance research in the local institutions.

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