THE DESIGN, FABRICATION AND APPLICATION OF CAPACITANCE-VOLTAGE (C-V) METER

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ABSTRACT

The parameters of modern semiconductor devices depends on the characteristics of the semiconductor surfaces, interfaces and on the distribution of impurities at the p-n junctions. A study is presented here on the importance of these characteristics in modern devices. It is followed by an overview of the metal oxide semiconductor (MOS) systems.

The capacitance dependence on the biasing voltage technique is chosen as the most versatile measurement method amongst other methods. It is able to analyse the p-n junctions, the Schottky junctions and the semiconductor insulator interfaces. The theories related to this capacitance-voltage (C-V) measurement method are presented first. It is followed by a detailed analysis of more and more important semiconductor surfaces and interface behaviour in different configuration.

An instrument was designed and built to do the C-V measurement on metal-oxide-semiconductor (MOS) structures. The instrument is producing plus-zero-minus D.C. voltage to bias the MOS capacitor, giving the voltage function. The capacitance is measured by applying a small high frequency signal and the impedance of the capacitance is derived. The D.C. and A.C. components are appropriately separated. A built in generator supplies the A.C. voltage. After precision rectification, an analogue instrument or an X-Y plotter can record the capacitance value.